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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,005	06/20/2003	Makoto Kudo	81751.0061	5768

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EXAMINER	
LAI, VINCENT	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,005	KUDO, MAKOTO	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
Supervisory PRIMARY EXAMINER
GROUP 2100
AU 2181
5/12/2006

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Acknowledgement is made of the amendment to the title filed by the applicant on 17 March 2006.

2. Acknowledgement is made of the amendment to the abstract filed by the applicant on 17 March 2006.

3. Acknowledgement is made of the amendment to the specification filed by the applicant on 17 March 2006.

4. The drawings were received on 17 March 2006. The examiner accepts these drawings and thus previous objections to drawings no longer apply.

Priority

5. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). Certified copies of the priority documents have been received.

Information Disclosure Statement

6. The information disclosure statement (IDS) submitted on 4/22/2005 was considered by the examiner.

Specification

7. The disclosure is objected to because of the following informalities: There are missing references in the disclosure of numbered elements in the figures. Specifically, elements 30, 50, 104, 106, 108, and 110 in Figure 2; elements 350, and 360 in Figure 3; elements 48, 50, and 54 in Figure 4; elements 450, and 460 in Figure 5; elements 48, 50, and 54 in Figure 6; element 560 in Figure 7; and element 610 in Figure 9. It is suggested that the applicant review the figures to ensure all numbered items are referred to the in the disclosure.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-2, and 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Branigin (U.S. Patent # 5,655,096).

As per claim 1, Branigin discloses a data processing device using pipeline control, comprising:

an instruction queue in which a plurality of instruction codes are fetched (Column 11, lines 50-52);

a fetch address operation circuit which calculates a fetch address used to fetch an instruction code in the instruction queue (Column 71, lines 1-6);

a fetch circuit which fetches an instruction code that is read out based on the fetch address into the instruction queue (Column 60, lines 11-12); and

a branch information setting circuit which decodes a branch setting instruction which explicitly or implicitly implies information for specifying a branch address (A branch instruction would inherently explicitly or implicitly specify a branch address else the branch instruction be useless) and to a branch target address when the fetch address is a branch address after x-th instruction from the branch setting instruction (See column 88, lines 26-50: The description is of a BRANCH AND LINK instruction which delays a branch action and uses a GOTO instruction which then also is capable of creating a delayed branch), the branch information setting circuit (Column 62, lines 54-59) stores the branch address in a branch address storage register (Column 65, lines 18-32: Describes the steps associated with using a branch address), and stores the branch target address in a branch target address storage register (Column 65, lines 18-32), when the branch setting instruction is decoded (See column 65, lines 18-32: Since the address is available before execution, it must mean that it is stored during decode);

wherein the fetch address operation circuit includes a circuit which compares one

of a previous fetch address and an expected next fetch address with a value stored in the branch address storage register, and then determines whether or not to output a value stored in the branch target address storage register as a next fetch address, based on the comparison result (Column 88, lines 33-41: The determined results are conditional).

As per claim 2, Branigin discloses a data processing device using pipeline control, comprising:

an instruction queue in which a plurality of instruction codes are fetched (Column 11, lines 50-52);

a fetch address operation circuit which calculates a fetch address used to fetch an instruction code in the instruction queue (Column 71, lines 1-6);

a fetch circuit which fetches an instruction code that is read out based on the fetch address into the instruction queue(Column 60, lines 11-12); and

a branch information setting circuit which decodes a branch setting instruction which explicitly or implicitly implies information for specifying a branch address (A branch instruction would inherently explicitly or implicitly specify a branch address else the branch instruction be useless) and to a branch target address when the fetch address is a branch address after x-th instruction from the branch setting instruction (See column 88, lines 26-50: The description is of a BRANCH AND LINK instruction which delays a branch action and uses a GOTO instruction which then also is capable of

creating a delayed branch), the branch setting circuit stores the branch address in a branch address storage register (Column 65, lines 18-32), and the branch target address in a branch target address storage register (Column 65, lines 18-32), when the branch setting instruction is decoded (See column 65, lines 18-32: Since the address is available before execution, it must mean that it is stored during decode);

wherein the fetch address operation circuit includes a circuit which compares an expected next fetch address obtained by incrementing a value in a fetch program counter by one instruction length with a value stored in the branch address storage register, and then outputs a value stored in the branch target address storage register as a next fetch address when the expected next fetch address coincides with the value in the branch address storage register, or outputs the expected next fetch address as a next fetch address when the expected next fetch address does not coincide with the value in the branch address storage register (Column 88, lines 33-41: The results are determined depending if a branch is needed).

As per claim 13, Branigin discloses electronic equipment comprising:

the data processing device (Column 115, lines 3-10: Computer processor in a personal computer, etc);

means for receiving input data (Column 115, lines 3-10: All computer systems have means for receiving input data); and

means for outputting a result of processing the input data by the data processing device (Column 115, lines 3-10: All computer systems have a means for outputting results).

As per claim 14, Branigin discloses electronic equipment comprising:

the data processing device (Column 115, lines 3-10: Computer processor in a personal computer, etc);

means for receiving input data (Column 115, lines 3-10: All computer systems have means for receiving input data); and

means for outputting a result of processing the input data by the data processing device (Column 115, lines 3-10: All computer systems have a means for outputting results).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3-12, and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Branigin (U.S. Patent # 5,655,096) in view of Moore et al (U.S. Patent # 5,784,584).

As per claims 3-4, Branigin teaches the use of instructions, which includes a loop instruction that designates a loop count (Column 107, lines 25-30: Loop instructions with loop count is part of the vector instructions);

Branigin does not explicitly teach the use of loop instructions for the purpose of branch instructions or the storage of branch target address.

Moore et al teaches the branch information setting circuit decodes the loop instruction which instructs to repeat a branch to the branch target address the number of times equal to the loop count (Column 24, lines 39-43), and stores the loop count designated by the loop instruction (Column 14, lines 43-46: The loop count is stored explicitly in LOOP COUNT); and the fetch address operation circuit includes a circuit which outputs a value stored in the branch target address storage register as a next fetch address until the number of times the branch to the branch target address repeats reaches the loop count (Column 24, lines 39-43: The next instruction is ran until loop count is zero or the number of times the branch repeats reaches the loop count).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Branigin to include the use of loop instructions in conjunction with branch instructions and thereby storing branch target addresses for later use.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Branigin by the teachings of Moore et al, because the use of loops for branches, especially when done in hardware as taught by

Moore et al, is "faster than conventional software implementation<s>" (Moore et al, column 14, lines 62-64). Creating a faster system was a goal of Branigin in using vector instructions with loop counts/branching (Branigin, column 107, lines 25-30).

As per claims 5-8, Branigin teaches the use of vector instructions, which includes a loop instruction that designates a loop count (Column 107);

Branigin does not explicitly teach the use of loop instructions for the purpose of branch instructions or the storage of branch target address.

Moore et al teaches the branch information setting circuit decodes the loop instruction which instructs to repeat a branch to the branch target address the number of times equal to the loop count (Column 24, lines 39-43), and stores the loop count designated by the loop instruction (Column 14, lines 43-46); and the fetch address operation circuit includes a circuit which decrements a value set in the loop counter each time when a branch to the branch target address occurs (Column 24, lines 39-43), and outputs a value obtained by incrementing the branch address by one instruction length as a next fetch address when the value of the loop counter reaches zero (Column 24, lines 39-40: Can use the ULOOP-IF-ZERO instruction after ULOOP-UNTIL-DONE instruction).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Branigin to include the use of loop instructions in conjunction with branch instructions and thereby storing branch target addresses for later use.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Branigin by the teachings of Moore et al, because the use of loops for branches, especially when done in hardware as taught by Moore et al, is "faster than conventional software implementation<s>" (Moore et al, column 14, lines 62-64). Creating a faster system was a goal of Branigin in using vector instructions with loop counts/branching (Branigin, column 107, lines 25-30).

As per claims 9-12, Branigin teaches the use of vector instructions, which includes a loop instruction that designates a loop count (Column 107);

Branigin does not explicitly teach the use of loop instructions for the purpose of branch instructions or the storage of branch target address.

Moore et al teaches the loop instruction has the branch target address which is fixed relative to the loop instruction and also has no branch target address information in an operand (Column 24, lines 1-3: the instructions are already collected in a group); and the branch information setting circuit includes a circuit which calculates the value fixed relative to the loop instruction and stores the calculated value in the branch target address storage register (Column 14, lines 47-48: Loop instructions are placed into instruction registers, with the MICROLOOP code predetermined).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Branigin to include the use of loop instructions in conjunction with branch instructions and thereby storing branch target addresses for later use.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Branigin by the teachings of Moore et al, because the use of loops for branches, especially when done in hardware as taught by Moore et al, is "faster than conventional software implementation<s>" (Moore et al, column 14, lines 62-64). Creating a faster system was a goal of Branigin in using vector instructions with loop counts/branching (Branigin, column 107, lines 25-30).

As per claims 15-18, the claims are rejected by the same reasoning of the above 35 U.S.C. 102(b) rejections of claims 13-14 in view of Moore et al.

Response to Amendment

10. Amendments submitted do not correct all objections to the specification and those objections still stand.

11. Applicant's arguments filed on 17 March 2006 have been fully considered but they are not persuasive.

Applicant's claim that amendments to claims 1 and 2 overcome the references cited, namely U.S. Patent # 5,655,096 to Branigin.

The 35 USC 102(b) rejections above has been modified to account for the amendments made. Branigin has anticipated such an instruction and pertinent parts are cited above.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Lai
Examiner
Art Unit 2181

vl
May 11, 2006

Supervisor / FRITZ FLEMING
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